REMARKS/ARGUMENTS

In the Office Action mailed October 30, 2009, claims 1-20 were rejected. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. No claims are added or canceled.

For reference, claims 1, 5, 6, and 8 are amended. In particular, claim 1 is amended to recite signal selection circuitry including a Tag RAM unit to generate a hit signal indicative of an originally mapped way. Also, claim 1 is amended to recite the remapping means is configured to generate a hit' signal based on the hit signal from the Tag RAM unit, and the hit' signal is indicative of a remapped way. Claim 8 is amended to recite similar limitations. These amendments are supported, for example, by the subject matter illustrated in Figs. 3 and 4 and by the corresponding subject matter described in the specification at page 6, line 10, through page 7, line 24. Consequently, claims 5 and 6 are each amended to delete the reference to the Tag RAM unit. Also, claim 5 is further amended to recite the remapping means is arranged in series with the Tag RAM unit to receive the hit signal from the Tag RAM unit for use in generating the hit' signal indicative of the remapped way. This amendment is supported, for example, by the subject matter illustrated in Fig. 3 and by the corresponding subject matter described in the specification at page 6, line 10, through page 7, line 2. Also, claim 6 is further amended to recite the remapping means is arranged in parallel to the Tag RAM unit to generate a plurality of remapped banks and ways corresponding to the input address, wherein the remapped banks and ways corresponding to the input address are generated independently of the hit signal from the Tag RAM unit and are subsequently processed together with the hit signal from the Tag RAM unit by selection logic to generate the hit' signal indicative of the remapped way. This amendment is supported, for example, by the subject matter illustrated in Fig. 4 and by the corresponding subject matter described in the specification at page 7, lines 5-24.

Claim Rejections under 35 U.S.C. 103

Claims 1-20 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Emma et al. (U.S. Pat. No. 5,584,002, hereinafter Emma)

Lasserre et al. (U.S. Pat. Pub. No. 2002/0065988, hereinafter Lasserre)

Asher (U.S. Pat. No. 6,671,822, hereinafter Asher)

Kramer (U.S. Pat. No. 4,868,869, hereinafter Kramer)

Swenson (U.S. Pat. No. 5,519,846, hereinafter Swenson)

In particular, claims 1, 2, 4, 5, 7-11, 14, 15, and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Emma in view of Lasserre. Claims 3, 13, and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Emma and Lasserre in further view of Asher. Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Emma and Lasserre in further view of Kramer. Claims 12 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Emma and Lasserre in view of Examiner's taking of Official Notice. Claims 19 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Emma and Lasserre in view of Swenson. However, Applicants respectfully submit that these claims are patentable over Emma, Lasserre, Asher, Kramer, Official Notice, and Swenson for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Emma and Lasserre because the combination of cited references does not teach all of the limitations of the claim. Claim 1 recites:

> An integrated circuit, comprising:
>
> at least one processing unit (PU);
>
> a cache memory (L2_bank) having a plurality of memory modules for caching data, wherein the cache memory comprises a plurality of distinct physical banks, wherein each physical bank comprises some of the memory modules and is configured to facilitate serving a read/write request independently of other physical banks to allow concurrent transfers for at least two of the physical banks; and
>
> signal selection circuitry for identifying which data cached in said cache memory, wherein the signal selection circuitry comprises:
>
> a Tag RAM unit (TagRAM) to generate a hit signal based on an input address, wherein the hit signal is indicative of an

originally mapped way for data corresponding to the input address; and

remapping means (RM, MapRAM) for performing an unrestricted remapping within said plurality of memory modules, wherein the unrestricted remapping permits remapping the memory modules from a first physical bank of memory modules to a second physical bank of memory modules, wherein the remapping means is configured to generate a hit' signal based on the hit signal from the Tag RAM unit, wherein the hit' signal is indicative a remapped way for the data corresponding to the input address.

(Emphasis added.)

In contrast, the combination of Emma and Lasserre does not teach all of the limitations of the claim. In particular, the combination of cited references does not teach a Tag RAM unit which generates a hit signal indicative of an originally mapped way and remapping means which generates a hit' signal that is based on the hit signal (from the Tag RAM unit) and is indicative of a remapped way.

For reference, the reasoning in the Office Action relies on Emma as purportedly teaching a Tag RAM unit (Office Action, 10/30/09, page 5) and remapping means (Office Action, 10/30/09, pages 3-4). However, even if Emma were to teach a Tag RAM unit and remapping means in general, as asserted in the Office Action, Emma nevertheless does not teach the specific functionality recited in the claim of 1) generating a hit signal indicative of an originally mapped way, and 2) generating a hit' signal indicative of a remapped way, wherein the hit' signal is based on the hit signal.

Rather, Emma merely describes remapping congruence classes using a cache unit 200 with addressing information in a cache directory 210. It appears that the cache directory includes all of the information used in a single lookup operation. Consequently, even if the lookup operation were to result in a signal indicative of a remapped congruent class, Emma does not describe generating a hit signal indicative of an originally mapped way. Thus, Emma also fails to teach generating a hit' signal (indicative of the remapped way) based on the hit signal (indicative of the original way).

For the reasons presented above, the combination of Emma and Lasserre does not teach all of the limitations of the claim because the combination of cited references does not teach a Tag RAM unit which generates a hit signal indicative of an originally mapped

way and remapping means which generates a hit' signal that is based on the hit signal (from the Tag RAM unit) and is indicative of a remapped way, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Emma and Lasserre because the combination of cited references does not teach all of the limitations of the claim.

Independent Claim 8

Applicants respectfully assert independent claim 8 is patentable over the combination of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Claim 8 recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of claim 8 differs from the language of claim 1, and the scope of each claim should be interpreted independently of other claims, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 8.

Dependent Claims

Claims 2-7 and 9-20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 8. Applicants respectfully assert claims 2-7 and 9-20 are allowable based on allowable base claims. Additionally, each of claims 2-7 and 9-20 may be allowable for further reasons, as discussed below.

Claims 12 and 16

In regard to claims 12 and 16, Applicants respectfully submit that the rejections of these claims are improper because the reliance on Official Notice is improper. Consequently, Applicants respectfully traverse the Examiner's taking of Official Notice in the Office Action.

The MPEP provides very strict guidelines to limit the availability of Official Notice. In particular, the MPEP states it is not appropriate for the Examiner to take Official Notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. MPEP 2144.03(A). The MPEP also states it is never appropriate to rely solely

on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. MPEP 2144.03(A) (citing In re Zurko, 258 F.3d at 1385 (Fed. Cir. 2001)). Furthermore, if Official Notice is taken without providing documentary evidence, the basis of the Official Notice must be set forth explicitly. The Examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge. MPEP 2144.03(B) (citing In re Soli, 317 F.2d at 946 (CCPA 1963) and In re Chevenard, 139 F.2d at 713 (CCPA 1943)).

Here, the Examiner does not provide evidentiary support for the assertion of Official Notice. Moreover, the reasoning in the Office Action relies solely on the Official Notice as the principal evidence for the indicated limitations. No other support is provided. Therefore, the rejection based on Official Notice is improper because it relies on Official Notice without providing evidentiary support.

Furthermore, the Office Action fails to provide factual findings to support the rejection based on Official Notice. The Office Action merely concludes that the indicated subject matter is well-known. However, there is no discussion of the facts, if any, that the Examiner might rely on to form such conclusion. The MPEP is clear that factual findings must be provided in order to properly support a rejection based on Official Notice. Given that the Office Action provides no specific factual findings and no explanation of related technical and scientific reasoning, the rejection based on Official Notice is improper. Accordingly, Applicants respectfully traverse the Official Notice taken by the Examiner in the Office Action. Moreover, Applicants respectfully submit that the Office Action fails to establish a *prima facie* rejection for claims 12 and 16 because the Official Notice is improper.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

/mark a. wilson/

Date: February 1, 2010

Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111